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09/842,694	04/27/2001	Isao Kobayashi	35.C13077 DI	9229

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EXAMINER
MONDT, JOHANNES P

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 09/04/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/842,694	KOBAYASHI ET AL.	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 June 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 7-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 7-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

Amendment C file 6/5/2 and entered as Paper No. 7 is the basis for the current Office Action. "Response to Arguments" found below contains the examiner's response to the Remarks of Applicant in said Amendment C. In Amendment C all claims have been substantially amended, either directly through amendment of the independent claims 1 and 8 or indirectly through dependence on said independent claims 1 or 8. Therefore, said examiner's response is restricted to those aspects that are still relevant for the present claim set, i.e., the amended claims 1-3 and 7-10.

Response to Arguments

1. Applicant's arguments filed 6/5/2002 have been fully considered but they are not persuasive. In particular, the new limitations introduce elements into the invention that can be found in the Prior Art as Admitted by Applicant, namely injection blocking layers of only holes or electrons can be found as layers 3 and 5 in Figure 1, which, as pointed out in the previous Office Action of Paper No. 6 should be labeled "Prior Art" and is illustrated in Applicant's disclosure to clarify the Prior Art, as discussed in "Background of the Invention"; see in particular "Field of the Invention" page 2, line 19 and 22, for the introduction of p layer 3 and n layer 5; page 3, lines 26-27; and page 3, line 27 – page 4, lines 1-3. The context within which the above-cited discussion is given place said n and p layers squarely in the Prior Art as Admitted by Applicant. See, for instance, page 1, lines 5-9. In this Office Action the independent claims stand rejected over the originally cited primary reference in view of said Prior Art as Admitted by Applicant.

Neither the presence of a second insulating layer in the primary reference in addition to all the other elements cited in the first Office Action, nor the possible absence of the object of the invention in the cited art are relevant to the present device invention.

By the amendment of claim 9 prior art must be cited in view of the explicit statements of the possible positive and negative sign of V_{UB} in Takeda et al under modes other than idle mode.

Finally, although the examiner requested Figures 1-4 to be provided with the required "Prior Art" label, Applicant to date has not done so. His reference to Figures submitted April 25, 2001, is to Figures in which this "Prior Art" label is absent.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. ***Claims 1-3 and 9*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeda et al.(5,591,963) in view of Prior Art Admitted by Applicant. In particular,

Referring to Figs. 4B, 9 and 11A, and to column 7, lines 26-42, column 11, line 51 – column 12, line 4: Takeda et al teach a photoelectric converter comprising a photoelectric conversion element of a laminated structure comprising:

a first electrode layer 2;

a lower insulating layer 70 for blocking the passage of first and second carrier having different polarity from the first carrier;

a photoelectric conversion semiconductor layer 4;

an insulating layer 71 that by virtue of being an insulator blocks inter alia the injection of the first carrier to the photoelectric conversion layer 4;

a second electrode layer in the form of transparent upper electrode 6; and, with reference to Fig. 9:

a switching means for operating the voltage, said means in the sense of Applicants' disclosure, pages 17 – 18, namely: controlled in such a manner that the switch is connected to a negative power source $V_{UB}=(V_U - V_B)$ on the refresh side 115 (cf. column 11, lines 51-59), to a positive power source on the read or photoelectric conversion side 120 (cf. column 11, line 66 – column 12, line 4);

said switching means for operating the converter by switching through the following operation modes b) through c), in that order, to apply an electric field to each layer of the photoelectric element (cf. column 13, lines 52-60):

b) a refresh mode for refreshing the first carrier (i.e., either electrons or holes) accumulated in the photoelectric conversion element; and

c) a photoelectric conversion mode for generating pairs of the first carrier and second carrier in accordance with an amount of incident light to accumulate the first carrier.

Takeda et al do not necessarily teach the further limitation that the layer 71 should block either holes or electrons only. However, as admitted prior art Applicant

describes (see Figure 1) a photoelectric converter in which at the position of insulating layer 71 as taught by Takeda et al there is instead a semiconductor layer of second conductivity type, hence capable of selectively blocking the charge carriers of first conductivity type, which is the standard manner in which photoelectric converters have been designed, as admitted by Applicant (see Applicant's disclosure, "Background of the Invention", particularly "Field of the Invention" page 2, line 19 and 22, for the introduction of p layer 3 and n layer 5; page 3, lines 26-27; and page 3, line 27 – page 4, lines 1-3). *Motivation* for replacing layer 71 in Takeda et al with the n-layer of the disclosure is the ease with which said n layer can be made, namely by doping the upper sub-layer of the underlying intrinsic semiconductor layer 4 in Takeda et al (Figure 1, and column 1, line 41), thus ensuring a high-quality match between layers 4 and 71. The inventions can be easily *combined*, because it is easy to dope a substratum. *Success* in combining the inventions can therefore be *reasonably expected*.

While in the Example 2, Fig. 9, there is no explicit mention of an idling mode, it is obvious from Fig. 4B and the discussion of Example 1, specifically column 7, lines 40-42 that the essence of the idling mode (recess mode in Applicant's disclosure) in other embodiments of the invention by Takeda et al is present through this Example for the *obvious purpose* to have the option of setting $V_{UB} = 0$: because this mode pertains to the relaxation of the intrinsic semiconductor layer 4 to its natural state, this setting has the obvious purpose of emitting excess carriers, i.e., either holes or electrons (completely alternatively called second carrier), from the layer and hence from the photoelectric conversion element.

By combining the Examples 1 and 2 it would thus have been obvious to one of ordinary skills in the art to modify the invention at the time it was made so as to include the complete switching means as described in claim 1.

Therefore claim 1 is unpatentable over Takeda et al.

With regard to claim 2: as explained above, $V_{UB} = 0$ in the idling mode as taught by Takeda et al (the primary reference), while being positive in the photoelectric conversion mode; hence claim 2 does not distinguish over the prior art.

With regard to claim 3: in the idling mode by Takeda et al $V_{UB} = 0$, as mentioned just above. The idling mode as taught by the primary reference thus complies with the requirement according to claim 3 for the reset mode as well as for the idling mode, and, consequently, the idling mode can be thought of as being split time-wise in a reset mode followed by an idling mode both modes being in full compliance with the requirements of claim 3. Therefore, the further limitation defined by claim 3 does not distinguish over the prior art.

With regard to claim 9: the potential V_{UB} in the primary reference (Takeda et al), which corresponds to the potential V_{dg} as defined by Applicant, can adopt zero, positive and negative values (cf. column 9, line 58 – column 10, line 2). Therefore, the further limitation as defined by claim 9 does not distinguish over the prior art.

4. ***Claim 7*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Takeda et al and Prior Art as Admitted by Applicant as applied to claim 1, and further in view of

Furukawa et al (5,591,960) and Arita (4,740,710). As detailed above, claim 1 is unpatentable over Takeda et al in view of Prior Art as Admitted by Applicant.

Takeda et al do not specifically teach the application of the photoelectric converter such that a plurality of said photoelectric elements are arranged one-dimensionally or two-dimensionally with a switching element connected for each of the photoelectric conversion elements according to the further limitation of claim 7.

However, one- and two-dimensional arrays of photoelectric elements of this kind have long been known in the art of photoelectric converter systems, as witnessed by Furukawa et al, who teach a structure consisting of a combination of pluralities of photoelectric element array sections *for the purpose of obtaining a high level signal with low noise* (cf. column 4, lines 48-55) comprising a plurality of photoelectric conversion elements, arranged two-dimensionally (cf. column 6, lines 33-37) with a switching element connected for each of the photoelectric conversion elements (cf. column 6, lines 49-56) with all the photoelectric conversion elements being divided into a plurality of n blocs (n=3, the blocks being circuit sections 1002/1102, 2002/2102, and 4002/4102; cf. column 6, lines 49-59), a light signal of all the n x m photoelectric conversion elements (m being the number of photoelectric elements in each block; undefined in claim!) divided into n=3 blocks is output (inherent in any useful application of pluralities of photoelectric converters is their output) an intersection part of the matrix wiring, which when using the photoelectric converter essentially taught by Takeda et al and the Prior Art as admitted by Applicant would comprise a laminated structure in which at least a first electrode layer, an insulating layer, a semiconductor layer and a second electrode

layer are provided in this order. Furukawa et al do not necessarily teach that each layer of the laminated structure should be formed as prescribed by the further limitation of claim 7. However, *from a cost production point of view* it makes utter sense to form each said layer in this manner, because of ease of mass production; while Arita indeed teaches a photoelectric reading apparatus wherein a plurality of switches are each connected with one end of each of the photoelectric elements (diodes) (cf. column 7, lines 25-32 and Fig. 6). The teaching by Furukawa et al can be easily combined with the invention by Takeda et al, because creating arrays of photoelectric converters has long been considered standard in the art of photoelectric conversion apparatus, while

Motivation to include the teaching by Furukawa et al and Arita in the invention essentially taught by Takeda et al and Prior Art as Admitted by Applicant is the obvious advantage of high S/N ratio as obtained through including the teaching by Furukawa et al, and, furthermore, the obvious advantage of lower manufacturing cost as obtained through including the teaching by Arita.

It thus would have been obvious to one of ordinary skills in the art to modify the invention at the time it was made so as to include the further limitation of claim 7.

5. ***Claim 8*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Takeda et al (5,591,963) and Prior Art as admitted by Applicant and in view of Perez-Mendez (5,596,198). Referring to Figs. 9 and 11A, column 11, line 51 – column 12, line 4, and column 13, lines 7-18: Takeda et al teach a photoelectric converter comprising a photoelectric conversion element of a laminated structure comprising:

a first electrode layer 2;

a lower insulating layer 70 for blocking the passage of first and second carrier having different polarity from the first carrier;

a photoelectric conversion semiconductor layer 4;

an insulating layer 71 that by virtue of being an insulator (i.e., inherently) blocks inter alia the injection of the first carrier to the photoelectric conversion layer 4;

a second electrode layer in the form of transparent upper electrode 6; and

a switching means for operating the voltage, said means being exactly in the sense of Applicants' disclosure, pages 17 – 18, namely: controlled in such a manner that the switch is connected to a negative power source (V_U - V_B) on the refresh side 115 (cf. column 11, lines 51-59), to a positive power source on the read or photoelectric conversion side 120 (cf. column 11, line 66 – column 12, line 4), or to GRN (ground) (cf. column 11, lines 60-65);

a switching means for operating the voltage, said means in the sense of Applicants' disclosure, pages 17 – 18, namely: controlled in such a manner that the switch is connected to a negative power source V_{UB}=(V_U - V_B) on the refresh side 115 (cf. column 11, lines 51-59), to a positive power source on the read or photoelectric conversion side 120 (cf. column 11, line 66 – column 12, line 4);

said switching means for operating the converter by switching through the following operation modes b) through c), in that order, to apply an electric field to each layer of the photoelectric element (cf. column 13, lines 52-60):

b) a refresh mode for refreshing the first carrier accumulated in the photoelectric conversion element; and

c) a photoelectric conversion mode for generating pairs of the first carrier and second carrier in accordance with an amount of incident light to accumulate the first carrier.

Takeda et al do not necessarily teach the further limitation that the layer 71 should block either holes or electrons only. However, as admitted prior art Applicant describes (see Figure 1) a photoelectric converter in which at the position of insulating layer 71 as taught by Takeda et al there is instead a semiconductor layer of second conductivity type, hence capable of selectively blocking the charge carriers of first conductivity type, which is the standard manner in which photoelectric converters have been designed, as admitted by Applicant (see Applicant's disclosure, "Background of the Invention", particularly "Field of the Invention" page 2, line 19 and 22, for the introduction of p layer 3 and n layer 5; page 3, lines 26-27; and page 3, line 27 – page 4, lines 1-3). *Motivation* for replacing layer 71 in Takeda et al with the n-layer of the disclosure is the ease with which said n layer can be made, namely by doping the upper sub-layer of the underlying intrinsic semiconductor layer 4 in Takeda et al (Figure 1, and column 1, line 41), thus ensuring a high-quality match between layers 4 and 71. The inventions can be easily *combined*, because it is easy to dope a substratum. *Success* in combining the inventions can therefore be *reasonably expected*.

While in the Example 2, Fig. 9, there is no explicit mention of an idling mode, it is obvious from Fig. 4B and the discussion of Example 1, specifically column 7, lines 40-

42 that the essence of the idling mode (recess mode in Applicant's disclosure) in other embodiments of the invention by Takeda et al is present through this Example for the obvious reason to have the option of setting $V_{UB} = 0$: because this mode pertains to the relaxation of the intrinsic semiconductor layer 4 to its natural state, this setting has the obvious purpose of emitting excess carriers from the layer and hence from the photoelectric conversion element.

Takeda et al do not necessarily teach the photoelectric converter to comprise a signal processing means, display means, electric transmission means and radiation source as further defined by claim 8.

However, the use of signal processing for the purpose of generating corresponding image signals to various peripherals, signal recording for video/data recorder use, signal display for interactive video display are standard in the art of photoelectric imaging, as shown for instance by Perez-Mendez (cf. column 6, lines 28-36). The examiner takes official notice that the use of electrical transmission for the transmission of data to other locations for remote processing or analysis is equally standard in the field. Finally, any photoelectric converter needs a radiation source for input, hence this aspect is inherent in a photoelectric converter system.

6. ***Claim 8*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Takeda et al and Prior Art as Admitted by Applicant and in view of Sashin et al (4,696,022). Referring to Figs. 9 and 11A, column 11, line 51 – column 12, line 4, and column 13,

lines 7-18: Takeda et al teach a photoelectric converter comprising a photoelectric conversion element of a laminated structure comprising:

a first electrode layer 2;

a lower insulating layer 70 for blocking the passage of first and second carrier having different polarity from the first carrier;

a photoelectric conversion semiconductor layer 4;

an insulating layer 71 that by virtue of being an insulator (i.e., inherently) blocks inter alia the injection of the first carrier to the photoelectric conversion layer 4;

a second electrode layer in the form of transparent upper electrode 6; and

a switching means for operating the voltage, said means being exactly in the sense of Applicants' disclosure, pages 17 – 18, namely: controlled in such a manner that the switch is connected to a negative power source (V_U - V_B) on the refresh side 115 (cf. column 11, lines 51-59), to a positive power source on the read or photoelectric conversion side 120 (cf. column 11, line 66 – column 12, line 4), or to GRN (ground) (cf. column 11, lines 60-65);

a switching means for operating the voltage, said means in the sense of Applicants' disclosure, pages 17 – 18, namely: controlled in such a manner that the switch is connected to a negative power source V_{UB}=(V_U - V_B) on the refresh side 115 (cf. column 11, lines 51-59), to a positive power source on the read or photoelectric conversion side 120 (cf. column 11, line 66 – column 12, line 4);

said switching means for operating the converter by switching through the following operation modes b) through c), in that order, to apply an electric field to each layer of the photoelectric element (cf. column 13, lines 52-60):

b) a refresh mode for refreshing the first carrier accumulated in the photoelectric conversion element; and

c) a photoelectric conversion mode for generating pairs of the first carrier and second carrier in accordance with an amount of incident light to accumulate the first carrier.

While in the Example 2, Fig. 9, there is no explicit mention of an idling mode, it is obvious from Fig. 4B and the discussion of Example 1, specifically column 7, lines 40-42 that the essence of the idling mode (recess mode in Applicant's disclosure) in other embodiments of the invention by Takeda et al is present through this Example for the obvious reason to have the option of setting $V_{UB} = 0$: because this mode pertains to the relaxation of the intrinsic semiconductor layer 4 to its natural state, this setting has the obvious purpose of emitting excess carriers from the layer and hence from the photoelectric conversion element.

Takeda et al do not necessarily teach the further limitation that the layer 71 should block either holes or electrons only. However, as admitted prior art Applicant describes (see Figure 1) a photoelectric converter in which at the position of insulating layer 71 as taught by Takeda et al there is instead a semiconductor layer of second conductivity type, hence capable of selectively blocking the charge carriers of first conductivity type, which is the standard manner in which photoelectric converters have

been designed, as admitted by Applicant (see Applicant's disclosure, "Background of the Invention", particularly "Field of the Invention" page 2, line 19 and 22, for the introduction of p layer 3 and n layer 5; page 3, lines 26-27; and page 3, line 27 – page 4, lines 1-3). *Motivation* for replacing layer 71 in Takeda et al with the n-layer of the disclosure is the ease with which said n layer can be made, namely by doping the upper sub-layer of the underlying intrinsic semiconductor layer 4 in Takeda et al (Figure 1, and column 1, line 41), thus ensuring a high-quality match between layers 4 and 71. The inventions can be easily *combined*, because it is easy to dope a substratum. *Success* in combining the inventions can therefore be *reasonably expected*.

Takeda et al do not necessarily teach the photoelectric converter to comprise a signal processing means, display means, electric transmission means and radiation source as further defined by claim 8. However, the use of signal processing for the purpose of generating corresponding image signals to various peripherals, signal recording for video/data recorder use, signal display for interactive video display are standard in the art of photoelectric imaging, as shown for instance by Sashin (4,179,100) (cf. Fig. 23 and column 15, line 64 – column 65, line 15). The examiner takes official notice that the use of electrical transmission for the transmission of data to other locations for remote processing or analysis is equally standard in the field. Finally, any photoelectric converter needs a radiation source for photon input, hence this aspect is inherent in a photoelectric converter system.

7. ***Claim 10** is rejected* under 35 U.S.C. 103(a) as being unpatentable over Takeda et al and Perez-Mendez, or, in the alternative, over Takeda et al and Sashin et al as applied claim 8 above, and further in view of Takeuchi et al (JP363250634A; no images available on the PTO Data Base). As detailed above, claim 8 is unpatentable over Takeda et al in view of Prior Art as Admitted by Applicant and Perez-Mendez, or, in the alternative, over Takeda et al in view of Prior Art as Admitted by Applicant and Sashin et al, none of whom, however, necessarily teach the use of phosphorus as a converter of wavelength of radiation as input into a photoelectric conversion element has long been known in the art as witnessed for instance by Japanese Patent to Takeuchi et al, who teach the conversion of X-rays to light in the visible range through the use of phosphorus prior to undergoing photoelectric conversion (cf. abstract and constitution), for the purpose of making it easier to read X-ray images through said conversion.

Motivation to include this teaching by Takeuchi et al is to reduce cost by making the system more easily operable (it is understood in the art that the radiation to be investigated for the case for which the invention by Takeuchi et al is intended, i.e., X-rays, is potentially a health risk). The teaching in this regard by Takeuchi et al can be easily *combined* with the invention of claim 8 through inclusion of a phosphorous or phosphorescent layer, which is standard in the light detection art. *Success* in combining the inventions can therefore be *reasonably expected.*

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
August 30, 2002

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800